

UNITED STATES PATENT APPLICATION

FOR

**SEMICONDUCTOR CHANNEL ON INSULATOR STRUCTURE**

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# SEMICONDUCTOR CHANNEL ON INSULATOR STRUCTURE

## BACKGROUND

### FIELD

[0001] Device structures.

### BACKGROUND

[0002] Transistors and other devices are connected together to form circuits, such as very large scale integrated circuits, ultra-large scale integrated circuits, memory, and other types of circuits. When the size of transistors, for example, is reduced and device compaction is increased, problems may arise concerning parasitic capacitance, off-state leakage, power consumption, and other characteristics of a device. Semiconductor on insulator (SOI) structures have been proposed in an attempt to overcome some of these problems. However, SOI structures generally have a high rate of defects, as it is difficult to produce thin, uniform semiconductor layers in fabrication. Defect problems in SOI structures include defects within a single wafer (e.g., the thickness of a wafer differs at various points on the wafer) and defects from wafer to wafer (e.g., an inconsistent mean silicon layer thickness among SOI wafers). As transistor devices are made smaller, channel length is generally reduced. Reduction in the channel length generally results in an increased device speed, as gate delay typically decreases. However, a number of side effects may arise when channel length is reduced. Such negative side effects may include, among others, increased off-state leakage current due to threshold voltage roll-off (e.g., short channel effects).

[0003] One way of increasing device speed is to use higher carrier mobility semiconductor materials to form the channel. Carrier mobility is generally a measure of the velocity at which carriers flow in a semiconductor material under an external unit electric field. In a transistor device, carrier mobility is a measure of the velocity at

which carriers (e.g., electrons and holes) flow through or across a device channel in an inversion layer. For example, higher carrier mobility has been found in narrow bandgap materials that include germanium (Ge). Germanium has electron and hole mobility of 3900 square centimeters per volt-seconds ( $\text{cm}^2/\text{Vsec}$ ) and 1900  $\text{cm}^2/\text{Vsec}$ , respectively, which are higher than that of electron and hole mobility of silicon, which are 1500  $\text{cm}^2/\text{Vsec}$  and 450  $\text{cm}^2/\text{Vsec}$ , respectively. The bandgap associated with a semiconductor material is generally based on the difference between the conduction band edge and valence band edge. Generally, higher mobility semiconductor materials have a narrower bandgap. With germanium, for example, the bandgap is approximately 0.67 electron-volts (eV), which is relatively small compared to that of silicon, which is approximately 1.1 eV.

[0004] For 300 millimeters (mm) wafers, it is difficult to grow a single crystal of high carrier mobility material. One way to use higher carrier mobility semiconductor materials in 300mm or larger wafer size device fabrication is to grow the material epitaxially on a 300mm or larger silicon carrier wafer. However, there is generally a large lattice mismatch between the high carrier mobility material and silicon. This large lattice mismatch tends to results in a high level of defects in the as grown epitaxial high mobility layer. One technique to reduce the defect density in the epitaxial layer is to introduce a graded buffer layer between the silicon carrier and the high carrier mobility material. By utilizing a graded buffer layer, the lattice parameter is varied in the buffer layer to serve as a transition between, for example, the silicon carrier to the higher carrier mobility epitaxial layer in a gradual fashion from the silicon material with a small or lower lattice mismatch being at the silicon interface and throughout the buffer layer. However, even though this graded buffer layer will tend to reduce some of the defects due to lattice mismatch, it is generally not sufficient to produce acceptable quality epitaxial layers for device applications.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Features, aspects, and advantages of embodiments will become more thoroughly apparent from the following detailed description, appended claims, and accompanying drawings in which:

[0006] **Figure 1** shows a cross-sectional side view of a portion of a structure including a semiconductor substrate having multiple dielectric layers formed thereon and a trench formed in ones of the dielectric layers.

[0007] **Figure 2** shows a top perspective view of the structure of **Figure 1**.

[0008] **Figure 3** shows the structure of **Figure 1** with a via formed in others of the dielectric layers through the trench.

[0009] **Figure 4** shows a top perspective view of the structure of **Figure 3**.

[0010] **Figure 5** shows the structure of **Figure 3** with a semiconductor material formed in the trench and via.

[0011] **Figure 6** shows the structure of **Figure 5** after a planarization to restrict the semiconductor material to the trench and via.

[0012] **Figure 7** shows the structure of **Figure 6** following the removal of ones of the dielectric layers to expose the semiconductor material of the trench.

[0013] **Figure 8** shows a top perspective view of the structure of **Figure 7**.

[0014] **Figure 9** shows the structure of **Figure 8** following the separation of a portion of the trench material from the via material.

[0015] **Figure 10** shows a cross-sectional side view through line A-A' of **Figure 9**.

## DETAILED DESCRIPTION

**[0016]** **Figure 1** shows a cross-sectional side view of a portion of a device structure. Device structure 100, in this embodiment, includes substrate 110. Substrate 110 includes a single crystal silicon substrate, such as portion 120 of 300 mm or larger single crystal silicon wafer. On portion 120 is graded epitaxial layer 130. In one embodiment, graded epitaxial layer is a high carrier mobility material such as silicon germanium (SiGe), gallium arsenide (GaAs), or indium antimony (InSb). In terms of a graded layer on portion 120 of silicon, epitaxial layer 130 has a relatively low lattice-mismatch film (e.g., a lattice mismatch less than one percent) nearest the portion 120 and the lattice mismatch generally increases in epitaxial layer 130 moving away from portion 120.

**[0017]** In the structure shown in **Figure 1**, overlying substrate 110 (on epitaxial layer 130) is first dielectric layer 140. In one embodiment, first dielectric layer 140 is an oxide (e.g., silicon dioxide ( $\text{SiO}_2$ )). First dielectric layer 140 is deposited to a thickness, as will become more clear later, that defects (e.g., dislocations) resulting from epitaxial layer 130 will terminate with first dielectric layer 140. Representatively, a layer of  $\text{SiO}_2$  can be deposited by chemical vapor deposition (CVD) or atomic layer deposition (ALD). Overlying first dielectric layer 140 in the structure of **Figure 1** is second dielectric layer 150. In one embodiment, second-dielectric layer 150 has an etch characteristic such that it may be etched (e.g., removed) selectively in the presence of first dielectric layer 140. In one embodiment, second dielectric layer 150 is silicon nitride ( $\text{Si}_3\text{N}_4$ ) deposited, for example, by CVD or ALD.

**[0018]** Overlying second dielectric layer 150 in the structure shown in **Figure 1** is third dielectric layer 160. In one embodiment, third dielectric layer 160 is a material that may be selectively etched (e.g., removed) in the presence of second dielectric layer 150. In one embodiment, third dielectric layer 160 is an oxide (e.g.,  $\text{SiO}_2$ ) deposited by CVD or ALD. As will be come more clear later, third dielectric layer 160 is deposited,

in one embodiment, to a thickness at least suitable as a thickness for a device channel (e.g., a transistor device channel). Third dielectric layer 160 of SiO<sub>2</sub> may be deposited, in one embodiment, by ALD to a thickness less than 100 angstroms (Å).

[0019] Overlying third dielectric layer 160 in the embodiment of a structure shown in **Figure 1** is fourth dielectric layer 170. In one embodiment fourth dielectric layer 170 has an etch characteristic such that it may be selectively etched (e.g., removed) in the presence of third dielectric layer 160. In one embodiment, fourth dielectric layer 170 is a silicon nitride (Si<sub>3</sub>N<sub>4</sub>) material deposited, for example, by CVD or ALD.

[0020] In the embodiment of the structure shown in **Figure 1**, trench 180 with trench pad 185 is formed in and/or through third dielectric layer 160 and fourth dielectric layer 170. In one embodiment, trench 180 and trench pad 185 may be formed using photolithographic techniques. For example, a masking material may define an exposed region or area of fourth dielectric layer 170 for trench 180 and trench pad 185. Suitably, trench 180 has a dimension suitable for at least a device channel (e.g., a transistor device channel) including a length, L<sub>1</sub>, and width, W<sub>1</sub>. Representatively, photolithographic techniques may be used to define a mask having an opening area suitable for forming a device channel (nanometer scale dimension). In one embodiment, trench pad 185 is selected to have an area (L<sub>2</sub> x W<sub>2</sub>) sufficient to provide area for the formation of a via in an area (base) of trench pad 185 (i.e., through second dielectric layer 150 and first dielectric layer 140). In one embodiment, a feature size of trench 180 is selected to be minimized (e.g., feature size defined by width, W<sub>1</sub>), so trench pad 185 has a width, W<sub>2</sub>, greater than width, W<sub>1</sub> of trench 180. Trench pad 185 has, in this embodiment, a length, L<sub>2</sub>, sufficient to provide area for a subsequent via.

[0021] To form trench 180 and trench pad 185, an etch chemistry suitable for etching silicon nitride (e.g., a CF<sub>4</sub>/O<sub>2</sub> chemistry) may then be used to expose third dielectric layer 160. Following the removal of the channel region corresponding to fourth dielectric layer 170, an etch chemistry suitable for etching third dielectric layer

160 may be employed to further define trench 180 and trench pad 185 through third dielectric layer 160. A suitable chemistry for etching  $\text{SiO}_2$  to the exclusion of  $\text{Si}_3\text{N}_4$  (e.g., to stop on a second dielectric layer 150 of, for example,  $\text{Si}_3\text{N}_4$ ) is, for example,  $\text{CHF}_3/\text{O}_2$ . **Figure 2** shows a top perspective view of structure 100 showing trench 180 and trench pad 185 formed through fourth dielectric layer 170 and third dielectric layer 160. Following the formation of trench 180 and trench pad 185, any photolithographic mask used to define trench 180 and trench pad 185 may be removed.

[0022] **Figure 3** shows the structure of **Figure 1** following the formation of a via in trench 180 and trench pad 185. In one embodiment, via 190 may be formed by defining an opening through an exposed portion of second dielectric layer 150 (exposed in trench pad 185) through photolithographic techniques. An etch chemistry suitable for etching second dielectric layer 150 may then be utilized to remove a portion of second dielectric layer 150 corresponding to the via opening and expose first dielectric layer 140. Via 190 may be defined of a dimension suitable for crystal growth. An etch chemistry suitable for etching first dielectric layer 140 may then be used to further define via 190. An etch chemistry, in one embodiment, suitable for etching first dielectric layer 140 of  $\text{SiO}_2$  selectively relative to epitaxial layer 130 is, for example,  $\text{CHF}_3/\text{O}_2$ . Accordingly, via 190 is formed in an area defined by trench pad 185 through second dielectric layer 150 and first dielectric layer 140 and stops (terminates) at epitaxial layer 130. **Figure 4** shows a top perspective view of the structure of **Figure 3** showing via 190 formed trench pad 185 to epitaxial layer 130.

[0023] **Figure 5** shows structure 100 following the introduction of a semiconductor material in trench 180, trench pad 185 and via 190. **Figure 5** shows the structure of **Figure 3** following the introduction of semiconductor material into trench 180, trench pad 185 and via 190. In one embodiment, semiconductor material 200 is deposited as an amorphous, polycrystalline, or epitaxial layer of semiconductor material. Suitable semiconductor material includes silicon, or a high carrier mobility material such as SiGe, GaAs, or InSb material. Semiconductor material 200 may be deposited by chemical

vapor deposition or other techniques. As shown in **Figure 5**, in one embodiment, semiconductor material 200 is deposited to a thickness such that the material fills via 190 and trench 180 and overlies (as viewed) fourth dielectric layer 170.

**[0024]** In an embodiment where semiconductor material 200 is amorphous or polycrystalline when deposited, semiconductor material 200 is annealed such that a crystalline seed from epitaxial layer 130 grows through semiconductor material 200. In one embodiment, annealing conditions are selected such that crystalline growth begins in via 190 and spreads beyond via 190 into trench pad 185 and trench 180. Thus, epitaxial growth is progressive in that the growth occurs in via 190 initially then spreads through trench pad 185 and trench 180 and laterally grows within trench pad 185 and trench 180 and ultimately above trench 180. Thus, an amorphous or polycrystalline material may be converted to single crystalline with a suitable anneal. For example, when a silicon material is used for semiconductor material 200, it can be amorphous or polycrystalline when deposited on the dielectric surface. Here, the amorphous to polycrystalline transition occurs between a deposition temperature of 580°C to 590°C. Silicon is grown epitaxially directly on exposed Si area resulting in a single crystalline material with varied defect density. An anneal of silicon material at a temperature of 1000°C or greater will tend to crystallize the amorphous or polycrystalline Si into single crystalline material within via 190 and trench pad 185 and trench 180, as well as tend to reduce the as grown defect density.

**[0025]** In another embodiment, rather than depositing semiconductor material 200 as an amorphous or polycrystalline material, semiconductor material may be selectively deposited (e.g., by CVD or molecular beam epitaxy (MBE) techniques) at a single crystalline growth temperature (e.g., 800°C or greater for silicon) and grown, starting from via 190 with continued growth into trench pad 185 and trench 180. Following the growth, an optional final anneal at a higher temperature may be employed to reduce the defect density. The higher temperature anneal may be accomplished by rapid thermal,



spike anneal, or by a laser anneal to minimize the atomic interdiffusion to retain the chemical composition in the high mobility channel and the epitaxial buffer layer regions.

[0026] Following the deposition and optional anneal of semiconductor material 200, structure 100 is planarized to confine semiconductor material 200 to trench pad 185, trench 180 and via 190. **Figure 6** shows structure 100 following the planarization of the structure to restrict semiconductor material 200 to trench pad 185, trench 180 and via 190. In one embodiment, a polish, such as a chemical-mechanical polish may be used to planarize structure 100. In one embodiment, semiconductor material 200 in trench 180 is planarized to a thickness such that it may be suitable as a device channel for a device ultimately formed in/on semiconductor material 200. Following the planarization, a surface cleaning is done with a optional anneal to create a high quality semiconductor surface in trench 180 for device fabrication.

[0027] **Figure 7** shows structure of **Figure 6** following the removal of fourth dielectric layer 170 and third dielectric layer 160. Fourth dielectric layer 170 may be removed by etch techniques, for example, utilizing an etchant suitable for removing fourth dielectric layer 170 (e.g.,  $\text{Si}_3\text{N}_4$ ) to the exclusion of semiconductor material 200 (e.g., phosphorus acid for  $\text{Si}_3\text{N}_4$ ). Following the removal of fourth dielectric layer 170, third dielectric layer 160 may be removed, again using an etch chemistry suitable for removing third dielectric layer 160 to the exclusion of semiconductor material 200 (e.g., a hydrogen fluoride chemistry for  $\text{SiO}_2$ ). **Figure 7** shows the structure including semiconductor material 200, the trench portion of semiconductor material 200, exposed on a surface of structure 100 (a top surface as viewed). **Figure 8** shows a top, perspective view of the structure of **Figure 7** and shows semiconductor material 200 formed in what was trench 180, trench pad 185 and via 190 of previously illustrated structure 100 (see **Figure 3** and **Figure 4**).

[0028] **Figure 9** shows the structure of **Figure 8** following the separation of a portion of semiconductor material 200 from the portion that includes semiconductor

material 200 within via 190 and a portion of trench pad 185 including, but not limited to, the entire portion. Referring to **Figure 9**, structure 100 includes semiconductor material 200 defined as semiconductor portion 200A and semiconductor portion 200B. Semiconductor portion 200B is separated at reference numeral 218 from semiconductor portion 200A which includes semiconductor material in via 190. Photolithographic/etch techniques may be used to separate semiconductor portion 200A and semiconductor portion 200B. In this manner, semiconductor portion 200B may be used as a channel for device formation and semiconductor portion 200A isolated. One reason to separate a portion of the semiconductor material that includes the portion extending through the via is that that portion containing epitaxial layer 130 is electrically disconnected from semiconductor portion 200B. Thus, where the first dielectric layer 160 is a dielectric material such as SiO<sub>2</sub>, that portion of structure 100 including semiconductor portion 200B is a semiconductor on insulated (SOI) structure, with semiconductor portion 200B serving as a device channel. Semiconductor portion 200B has a length,  $L_0$ , that, in one embodiment, is less than  $L_1$ .

**[0029]** **Figure 10** shows the structure of **Figure 9** through a cross-section through lines A-A' of **Figure 9**. In this representative embodiment, a transistor device is formed in/on semiconductor portion 200B. Representatively, the transistor device includes gate electrode 220 on semiconductor portion 200B (separated by a dielectric material) and source junction 230 and drain junction 240 formed in semiconductor portion 200B.

**[0030]** In the above embodiments, various dielectric layers have been described in forming an SOI structure. It is appreciated that the designation of first through fourth dielectric layers are for convenience and should not be understood to limit the subject matter described in the claims. Thus, for example, although four dielectric layers are described, it is appreciated that one or more may be combined into a single or multiple dielectric layers. Alternatively, more than four dielectric layers may be used to define a structure. It is appreciated that the various layers formed on structure 100 to define a

device channel need not each be (or all be) dielectric material layers. Although an SOI structure is formed (requiring, for example, second dielectric layer 150 and perhaps first dielectric layer 140), for similar or other structures the various layers (particularly third dielectric layer 160 and fourth dielectric layer 170) may be formed of other suitable materials since the layers may be sacrificial in the sense that they may be removed to form an ultimate device structure. The embodiments described take advantage of the deposit and etch techniques of dielectric materials such as  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$ . Such techniques allow the fabrication of small critical dimension (CD) structures such as channel structures and the control of the channel thickness (through trench depth). Further, the defect density associated with semiconductor materials having different lattice structures may be controlled again by the thickness of dielectric layer material (via depth).

[0031] In the preceding paragraphs, specific embodiments are described. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.